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International Review of Electrical Engineering (IREE)

PART B

Contents:

(continued from Part A)

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International Review of Electrical Engineering (I.R.E.E.), Vol. 5, N. 6
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Improvement of Power System Transient Stability Using TCBR and TCSC, a Comparative Study

Sabir Messalti[1,2], Saad Belkhiat[1], Shahrokh Saadate[2], Damien Flieller[2]

Abstract – *This paper shows the modeling and the effectiveness of two FACTS devices for transient stability improvement of power systems: The ability of flexible adjustment of Thyristor Control Breaking Resistor (TCBR) and Thyristor Controlled Series Capacitor (TCSC) can presumably increase the power systems stability. Their effect has been investigated separately and can be combined together to have a higher benefits when the power system is equipped with a compensator. Critical Clearing Time (CCT) has been used as an index for evaluated transient stability. The transient stability is assessed by the criterion of relative rotor angles, using Runge-Kutta method. The effectiveness of the proposed method is tested on the WSCC3 nine-bus system applied to the case of three-phase short circuit fault in one transmission line. The simulation results and their comparison are presented in this paper.*

Keywords: *Critical Clearing Time CCT, Transient Stability, Runge-Kutta Method, TCBR, TCSC*

Nomenclature

D_i	Damping constant of i^{th} generator
E'_{di}	d-axis transient emfs of i^{th} generator
E'_{qi}	q-axis transient emfs of i^{th} generator
H_i	Inertia constant of i^{th} generator
I_d	d-axis generator currents of i^{th} generator
I_q	q-axis generator currents of i^{th} generator
P_{mi}	Mechanical input power of i^{th} generator
P_{ei}	Electrical power of i^{th} generator
T'_{d0i}	d-axis transient time constants of i^{th} generator
T'_{q0i}	q-axis transient time constants of i^{th} generator
V_{ex}	Field voltage controlled by a voltage regulator of i^{th} generator
x'_{di}	d-axis generators' transient reactance of i^{th} generator
x'_{qi}	q-axis generators' transient reactance of i^{th} generator
δ_i	Rotor angle of i^{th} generator
ω_b	Rotating angular velocity
ω_i	Rotor angular velocity of i^{th} generator
R	Speed regulation
T_c , T_s	Time constants regulator
P_m	Mechanical power
$P_m(0)$	Initial mechanical power
P_1 , P_2	Intermediate state variables
DB_t	Dead band
K_R	Regulator gain
K_A	Amplifier gain
K_E	Exciter gain
K_F	Stabilizer gain
T_R	Time constant of regulator
T_A	Time constant of amplifier
T_E	Time constant of exciter
T_F	Time constant of stabilizer
V_1	Regulator output voltage
V_{or}	Initial amplifier output voltage
V_R	Amplifier output voltage
V_t	Stator voltage
V_2	Stabilizer output voltage
V_{di}	d-axis emfs of i^{th} generator
V_{qi}	d-axis emfs of i^{th} generator
B	Shunt susceptance of the line
G	Shunt conductance of the line

I. Introduction

Modern power systems are very complex and interconnected. The great need to improve the quality of electrical power requires to keep the reliability and the stability of electrical system. Furthermore, the demand for electrical energy around the world increases continuously while the expansion of power generation

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Voltage Sag Compensation in Distribution System Due to SLG Fault Using D-STATCOM

Hendri Masdi[1], Norman Mariun[1], S. M. Bashi[1], Azah Mohamed[2]

Abstract – *This paper presents the distribution static compensator (D-STATCOM) for load compensation in an unbalanced distribution system. Simulation were carried out for both cases where, D-STATCOM was connected to the system and not, with simulation interval 0.20 sec. In order to verify the simulation results, a prototype D-STATCOM is constructed and connected in shunt load. Single Line to Ground (SLG) fault is tested on the load and the corresponding results without and with D-STATCOM are recorded then the experimental results obtained from the constructed D-STATCOM are compared with the simulation results. The aim of the D-STATCOM here is to provide voltage regulation at the load point and mitigate the voltage sag generated when the fault occurred. The D-STATCOM is intended to replace the widely used static var compensator (SVC). The compensation scheme of the D-STATCOM is derived using the symmetrical component method. In this work, the 12-pulse D-STATCOM configuration with IGBT has been designed and the graphic based models of the D-STATCOM have been developed using the PSCAD/EMTDC4.2 electromagnetic transient simulation program.* **Copyright © 2010 Praise Worthy Prize S.r.l. - All rights reserved.**

Keywords: *SLG, D-STATCOM, Voltage Sag Compensation*

I. Introduction

Electric problems always occur regardless of time and place. This may cause an impact to the electric supply thus may affect the manufacturing industry and impede the economic development in a country. The major electric problems that always occur in power systems are the power quality problems that have been discussed by the electrical engineers around the world, since problems have become a major issue due to the rapid development of sophisticated and sensitive equipment in the manufacturing and production industries.

The increased concern for power quality has resulted in measuring power quality variations, studying the characteristics of power disturbances and providing solutions to the power quality problems [7].

In distribution systems, the power quality problems can reduce the power supplied to the customers from its nominal value. Voltage sag, harmonic, transient, overvoltage and undervoltage are major impacts to a distribution system. The utility and the users are responsible in polluting the supply network due to operating of large loads.

Environmental effects also give an impact to the power quality and its reliability. Major concerns on industrial power quality problems are that they affect the production, due to sensitive equipment in the industries. Where there are power quality problems, equipment may misoperate or machine may possibly shut down.

Voltage sags is the most important power quality problems faced by many industries and utilities. It contributes more than 80% of power quality (PQ) problems that exist in power systems [12]. By definition, a voltage sag is an rms (root mean square) reduction in the AC voltage at the power frequency, for duration from a half-cycle to a few seconds [6]. Voltage sags are not tolerated by sensitive equipments used in modern industrial plants such as process controllers, programmable logic controllers (PLC), adjustable speed drive (ASD) and robotics [12]. It has been reported that, high intensity discharge lamps used for industrial illumination get extinguished at voltage sags of 20% and industrial equipments like PLC and ASD are about 10% [9].

Various methods have been applied to reduce or mitigate voltage sags. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing uninterruptible power supplies (UPS). However, the PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. The D-STATCOM has emerged as a promising device to provide not only for voltage sags mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction and harmonic control [4],[13]. The D-STATCOM has additional capability to sustain reactive current at low voltage, reduce land use and can be developed as a

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voltage and frequency support by replacing capacitors with batteries as energy storage [10].

There are many solutions in mitigating the power quality problems at a distribution system such as using surge arresters, active power filters, isolation transformer, uninterruptible power supply and static VAR compensator. [1] proposed a new D-STATCOM control algorithm which enables separate control of positive and negative sequence currents and decoupled control of d- and q-axes current components. [3] use real time digital simulation of power electronic system which is a heavily computer intensive operation, and based on VSC D-STATCOM power system. From the studies, it is shown that all these equipments are capable in solving power quality problems. The best equipment to solve this problem at distribution systems at minimum cost is by using Custom Power family of D-STATCOM.

In this paper, D-STATCOM for voltage sag compensation in an SLG faults distribution system is explained. The designed D-STATCOM is connected in shunt to the 11 kV test distribution system. Passive filters will be employed to reduce the harmonics present in the output of the D-STATCOM which exceed the limits by IEEE standards. Simulation results on the performance of the D-STATCOM for voltage sag mitigation are presented and compared with the experimental results.

II. Materials and Methods

II.1. Basic Configuration and Operation of D-STATCOM

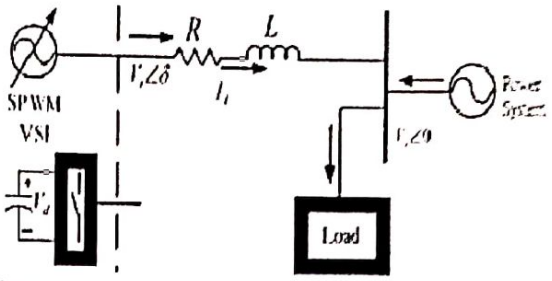
The D-STATCOM is a three-phase and shunt connected power electronics based device. It is connected near the load at the distribution systems. The major components of a D-STATCOM are shown in Fig. 1. It consists of a dc capacitor, three-phase inverter (IGBT, thyristor) module, ac filter, coupling transformer and a control strategy [10].

The basic electronic block of the D-STATCOM is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency.

The D-STACOM employs an inverter to convert the DC link voltage V_{dc} on the capacitor to a voltage source of adjustable magnitude and phase. Therefore the D-STATCOM can be treated as a voltage-controlled source. The D-STATCOM can also be seen as a current-controlled source. Fig. 1 shows the inductance L and resistance R which represent the equivalent circuit elements of the step-down transformer and the inverter will is the main component of the D-STATCOM.

The voltage V_i is the effective output voltage of the D-STATCOM and δ is the power angle.

The reactive power output of the D-STATCOM inductive or capacitive depending can be either on the operation mode of the D-STATCOM.



where:
V_s = Peak phase voltage
I_L = Step – drop of load current
Vi = Inverter output voltage
V_{DC} = Capacitor voltage
VSI = Voltage source inverter
$SPWM$ = Sinusoidal PWM
L = Inductance system
R = Resistance system

Fig. 1. Basic Building Blocks of the D-STATCOM

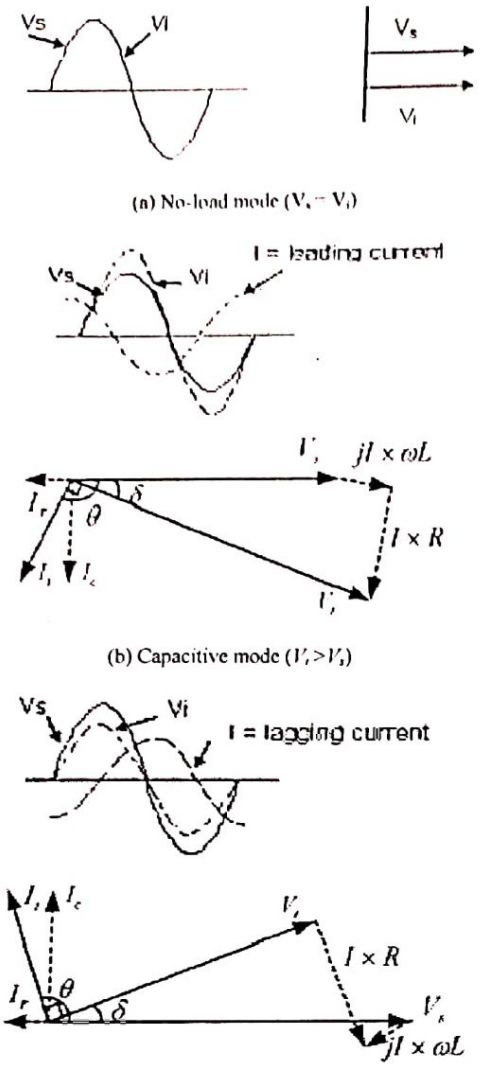
Referring to Fig. 1, the construction controller of the D-STATCOM is used to operate the inverter in such a way that the phase angle between the inverter voltage and the line voltage is dynamically adjusted so that the D-STATCOM generates or absorbs the desired VAR at the point of connection. The phase of the output voltage of the IGBT-based inverter, V_i, is controlled in the same way as the distribution system voltage, V_s.

Figs. 2 show the three basic operation modes of the D-STATCOM output current, I, which varies depending upon V_i. If V_i is equal to V_s, the reactive power is zero and the D-STATCOM does not generate or absorb reactive power. When V_i is greater than V_s, the D-STATCOM shows an inductive reactance connected at its terminal. The current, I, flows through the transformer reactance from the D-STATCOM to the ac system, and the device generates capacitive reactive power. If V_s is greater than V_i, the D-STATCOM shows the system as a capacitive reactance. Then the current flows from the ac system to the D-STATCOM, resulting in the device absorbing inductive reactive power [4].

II.2. Construction Of The 12-Pulse D-STATCOM and Control System

Fig. 3 shows a typical 12-pulse inverter arrangement utilizing two transformers with their primaries connected in series [5]. The first inverter is connected to the system through a Y-Y arrangement, whereas a Y-Δ connection is used for the second inverter.

Each inverter operates as a 6-pulse inverter, with the Y-Δ inverter being delayed by 30^0 with respect to the Y-Y inverter. The current flowing into each inverter is the same, scaled by the transformer ratio, as the current being drawn from the system by the D-STATCOM. For the Y-Δ inverter, the current is also delayed by 30^0 with respect to the current of the Y-Y inverter [5].



Figs. 2. Operation modes of D-STATCOM

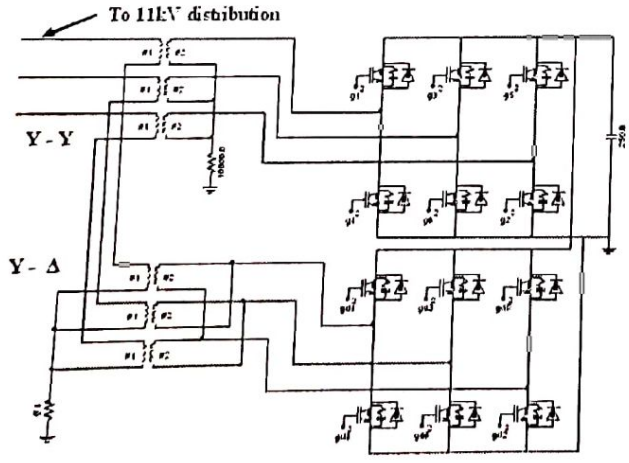


Fig. 3. The 12-pulse D-STATCOM arrangement

Fig. 3 also shows the proposed 12-pulse D-STATCOM configuration with the IGBT's used as power devices. The IGBTs are connected anti parallel with diodes for commutation purposes and charging of the DC capacitor [2].

The DC side of D-STATCOM is connected in parallel to keep the voltage on the DC side as low as possible and to improve utilization of the DC side capacitor. The first transformer is in wye-to-wye connection and the second transformer is in wye-to-delta connection. This is to give a 30^0 phase shift between the pulses and to reduce harmonics generated from the D-STATCOM. Both transformers are stepped down from 11kV to 2kV, i.e. 11:2 transformers. The D-STATCOM is connected in shunt to the system.

II.3. Inverter Design

Inverters are used to convert DC signal to AC signal. In this work a 3-phase inverter has been developed. The DC source in the system is the DC capacitor. This is located in parallel with the D-STATCOM.

The charging of the capacitor is referred to the reactive power in the system. The capacitor is charged when the current in the system is higher than in the D-STATCOM and is discharged when the current is lower. For inverter the most important part is the sequences of operation of the IGBTs. The IGBTs signals are referred to the Sinusoidal Pulse Width Modulation (SPWM) that will generate the pulses for the firing of the IGBTs. Fig. 4 shows the modeling of the inverter.

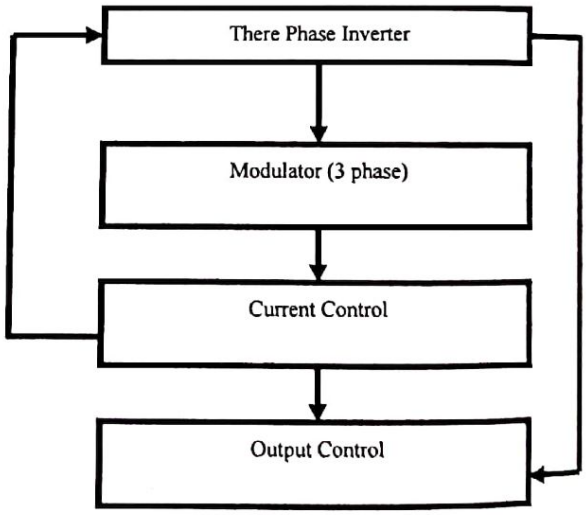


Fig. 4. Modeling of Inverter

II.4. Capacitor Sizing

Capacitor sizing is referred to the fault current in the system. The difference in current between the current before and after the fault is considered as current faults. In capacitor sizing, a suitable range of DC capacitor is needed to store the energy to mitigate the voltage sag. The DC capacitor, C_{DC} is used to inject reactive power to

the D-STATCOM when the voltage is in sag condition. In the design, the harmonic effects must be considered because the load is inductive and this may affect the value of C_{DC}. The following equation is used to calculate C_{DC} [2]:

$$\frac{1}{2} C_{DC} \cdot [V_{CMAX}^2 - V_{DC}^2] = \frac{1}{2} V_{SM} \cdot \Delta I_L \cdot T \quad (1)$$

Equation (1) is used for harmonic mitigation in single phase system but for a three phase system the equation is given by:

$$C_{DC} = 3 \times \frac{V_S \cdot \Delta I_L \cdot T}{V_{C_{max}}^2 - V_{DC}^2} \quad (2)$$

where:

V_S = Peak phase voltage
I_L = Step – drop of load current
T = Period of one cycle of voltage and current
V_{CMAX} = Pre-set upper limit of the energy storage C (per-phase),
V_{DC} = Voltage across C (per-phase)

The value of ΔI_L can be found by measuring the load current before and during the voltage sag [2].

The value of V_{DC} is given by:

$$V_{DC} = \frac{3\sqrt{3} \cdot V_s \cdot \cos\alpha}{\pi} \quad (3)$$

where α = delay angle.

If $\alpha = 0$, the equation become:

$$V_{DC} = \frac{3\sqrt{3} \cdot V_s}{\pi} \quad (4)$$

The value of V_{CMAX} is the present upper limit of C_{DC}, and is two or three times of the V_{DC}.

II.5. Transformer Configuration

For the 12-pulse operation, two six-pulse inverters that are shifted by 30^0 from each other can provide the phase angle shift for a suitable configuration. For the 12-pulse D-STATCOM, the transformers are connected in parallel to each other for six pulse arrangement. The first inverter is connected in Y-Y to the system lagging 30^0 from the second inverter which is connected in Y-Δ arrangement to the system. For Y-Δ connection, it will provide a phase shift of about 30^0. This phase shift is needed to make sure the operation of the 12 pulse D-STATCOM is in a stable condition.

II.6. Controller Configuration

The control used in the simulation is AC voltage control or reactive power control. This control is divided into two parts, that is, the SPWM and reactive power control. Fig. 5 shows that the microcontroller regulates the AC side voltage sourced converter (VSC) or alternatively, reactive power into or out of the VSC. The output of micro controller is the angle order, which is used to maintain the phase shift.

The reactive power flow from the system is compared to the reference per-unit voltage that contributes to a change of the phase shift. The difference in phase shift will provide the needed reactive power from the DC capacitor.

The SPWM technique is described in Fig. 6 and Fig. 7. The SPWM firing pulse to the IGBTs are obtained by comparing the PWM carrier signals and the reference sine waveform. The phase locked loop (PLL) plays an important role in synchronizing the switching to the distribution system voltage and lock to the phase at fundamental frequency to generate the PWM triangular carrier signals.

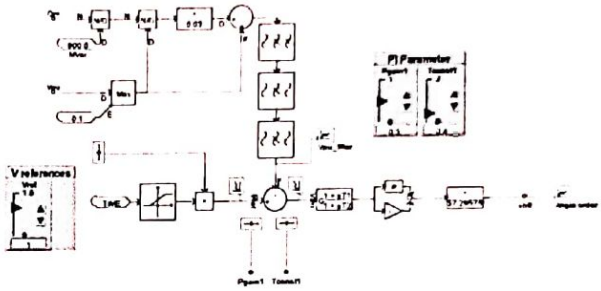


Fig. 5. Reactive power Control Loop

The frequency is multiplied with PWM switching frequency. As shown in Figs. 8, the switching frequency is set at 1.5 kHz, which is 30 times the system operating frequency, and converted to a triangular signal whose amplitude is fixed between –1 to +1. In Fig. 7, the pulses PLL are applied to generate sinusoidal curves at the wanted fundamental frequency. A shift is effectively the output coming from the reactive power control loop, i.e. the angle order. The difference in angle order will change the width of the PWM signal and ultimately the needed reactive power to be supplied to the system.

In this simulation, the amplitude is fixed and phase shift is control to maintain at 30^0.

Figs. 8 show the output of a triggering signal of IGBT when voltage sag occurs in the system.

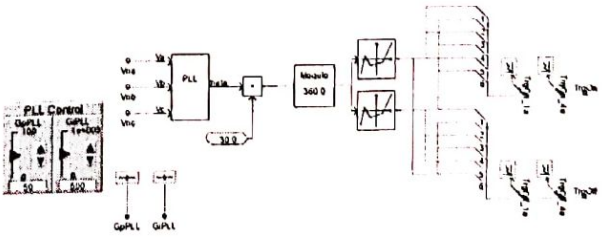


Fig. 6. SPWM Carrier Signal

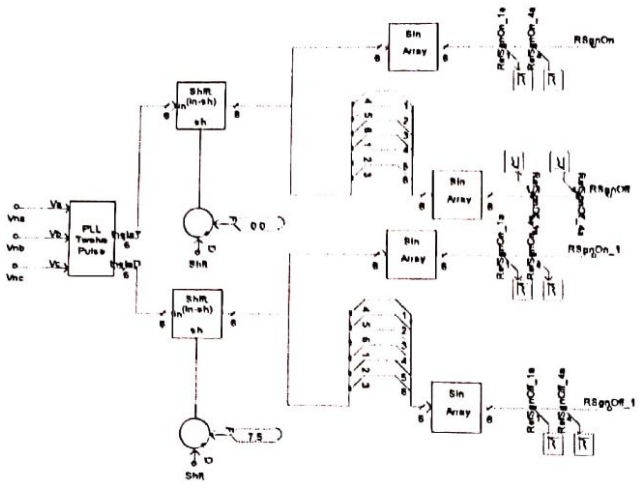
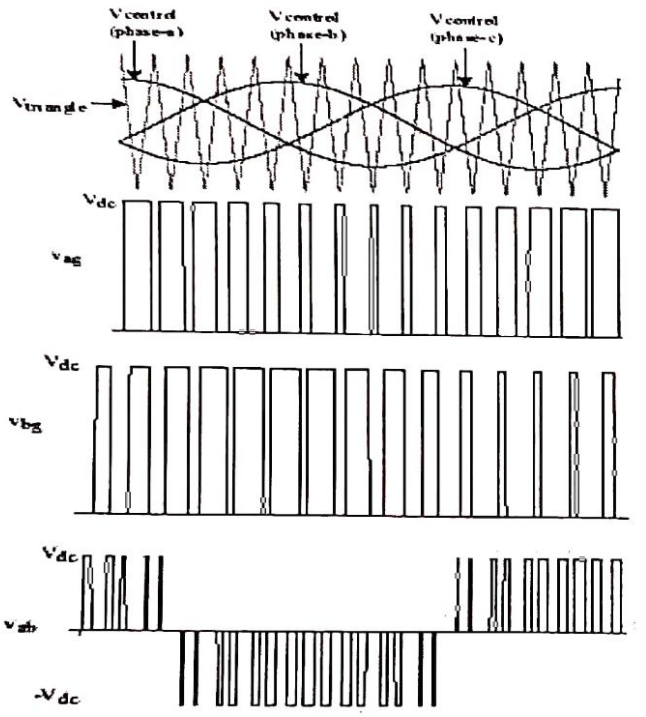
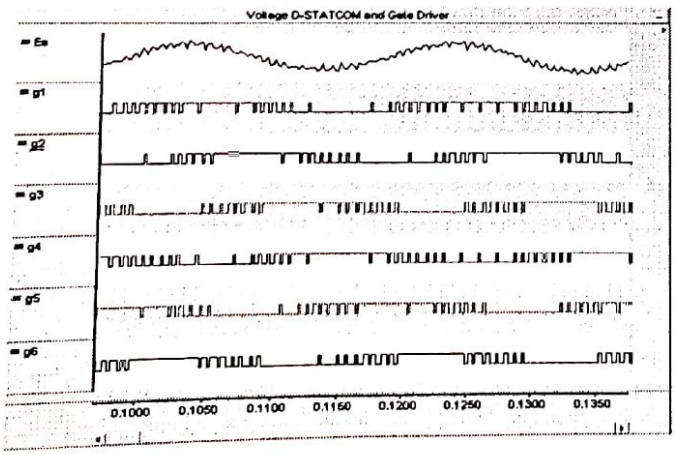


Fig. 7. Generation of Reference Sine wave



(a) Fundamental



(b) Simulation

Figs. 8. Simulation of SPWM for IGBT gate drive

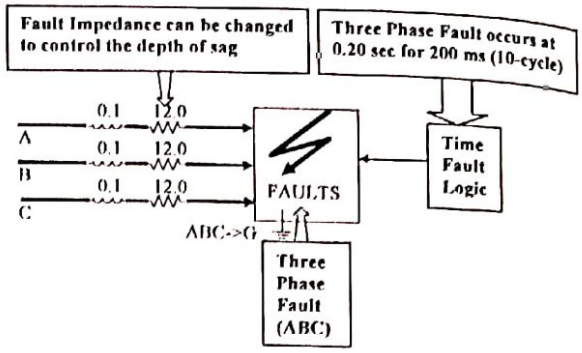


Fig. 9. Three-phase Fault Component to Introduce Voltage Sag

III. Results and Discussion

III.1. Simulation Voltage Sag Condition Results

In the simulation study, a voltage sag in the system is created by the three-phase fault component from the PSCAD/EMTDC software's library.

Fig. 9 shows the component applied to generate voltage sag. The system was simulated for 0.8 seconds with a three-phase balanced fault occurring at time 0.4 sec for a duration of 0.2 s. Figure 10 shows the per-unit voltage, current and voltage profiles of the system. From Fig. 11, it can be seen that due to the SLG fault, voltage sag has occurred. The depth of sag can be changed by changing the fault impedance in Real and Reactive Power.

The percentage of sag for the system is calculated using the following equation:

$$Sag(\%) = \frac{V_{pre-sag}(p.u) - V_{sag}(p.u)}{V_{pre-sag}(p.u)} \times 100 = \frac{0.818 - 0.498}{0.818} \times 100 = 39.12\% \quad (5)$$

It is evident from the graphs shown in Figure 11 and Figures 12 that the line current, $I_{L\text{-}L}$ (rms), dropped from 89A to 62A, harmonic load (source) and the line voltage, $V_{L\text{-}L}$, dropped from 7.344kV to 4.97kV. From these values, the DC capacitor value is determined as follows (equation (2)):

$$C_{DC} = 3 \times \frac{V_s \cdot \Delta I_L \cdot T}{V_{C_{max}}^2 - V_{DC}^2} \quad (6)$$

where, in this case for V_S = 1633 V, I_L = 148.5A, T = 20ms, $V_{C_{max}}$ = 8400V and V_{DC} = 2000V, the calculated capacitance value is $C_{DC} \approx 220\mu F$.

The VAR rating of the D-STATCOM when C_{DC}=220μF is calculated as:

$$VAR = 314.2 \times C_{DC} \times V_{L-L}^2 \quad (7)$$

V_{LL} is the nominal line-to-line voltage of the system at the point of connection of the filter. In this case, V_{LL} = 6.93 kV and the *VAR* rating of the D-STATCOM is 3.3 MVAr.

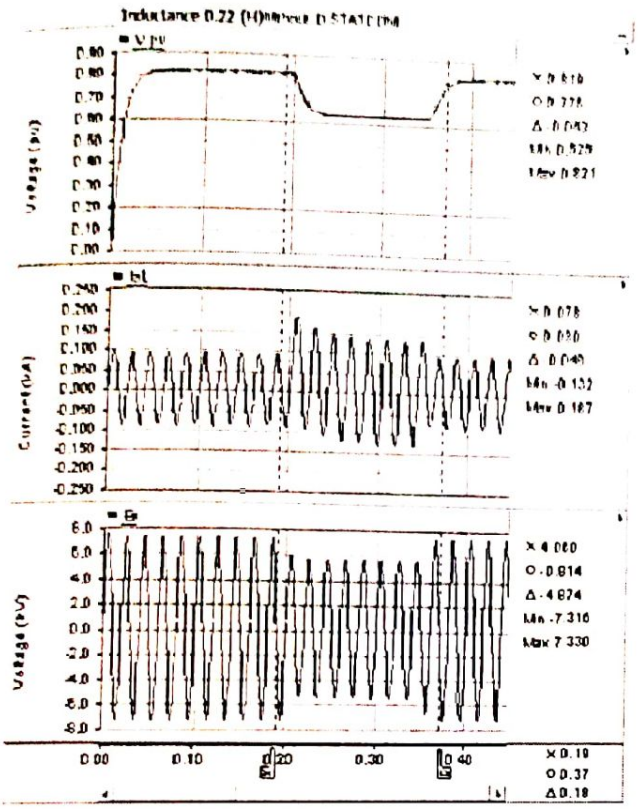


Fig. 10. Voltage (p.u), Current (kA), and Voltage(kV) of the System during Voltage Sag Condition

III.2. Simulation of Voltage Sag Mitigation by D-STATCOM

The D-STATCOM is now connected in shunt with the 11kV system and the simulation is set to run again for 0.8sec. The switching frequency of the SPWM control is set at 1.65 kHz. Figs. 12 ((a), (b), and (c) show the results obtained from the simulation. From Figs. 12, it can be seen that the system's per unit voltage is maintained at 1.0 p.u. The spikes at the beginning and end of sag are due to capacitor charging and discharging. Figs. 12 show the duration of voltage sag from 0.4s to 0.6s and during this period the D-STATCOM responds well to give the system better ride through capability. The sag was mitigated within 20ms and limited to less than 20% of sag before the system recovered to 1.0 p.u. Figs. 13 show that the D-STATCOM through the control feedback, the angle order is always kept at 30^0 between the 12 pulses. It can be seen that the DC current of the DC capacitor is fluctuating from negative to positive. This is due to the capacitor charging and discharging. The primary voltage of the 11:2 transformer, i.e. the system voltage, is maintained at about 11kV during the duration of sag. This proves that the D-STATCOM works very well in compensating the voltage sag caused by SLG faults and load (source) harmonics.

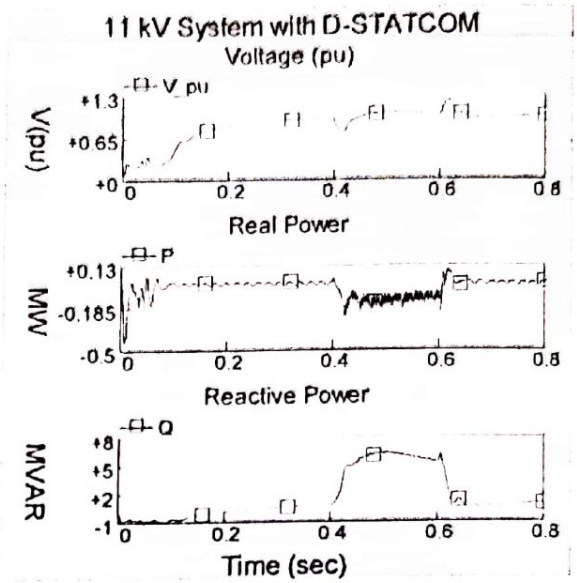
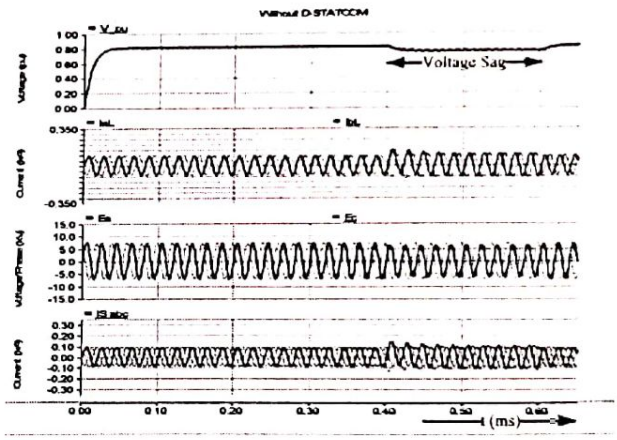
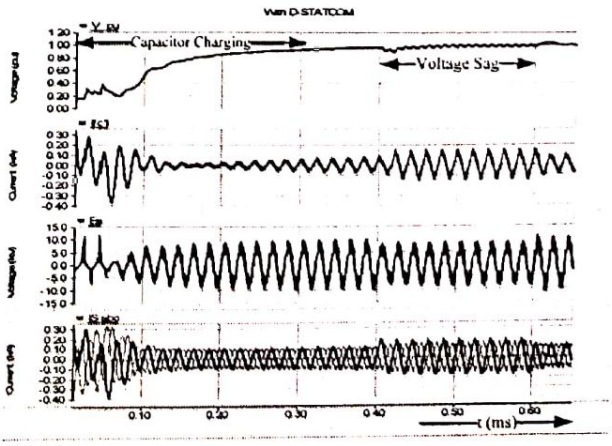


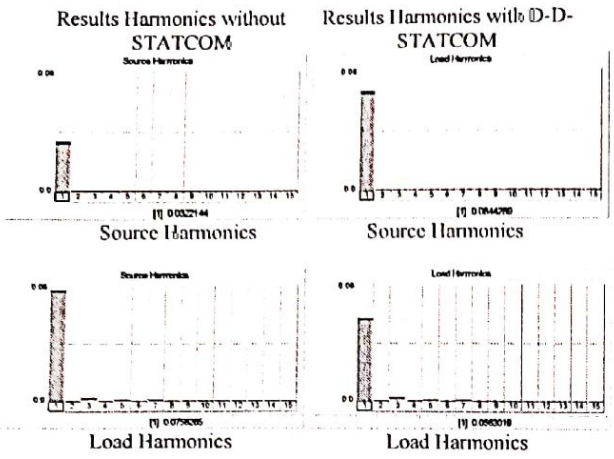
Fig. 11. 11kV System with D-STATCOM V (p.u), Real and Reactive Power



(a) Results of Voltage and Current without D-STATCOM



(b) Results of Voltage and Current with D-STATCOM



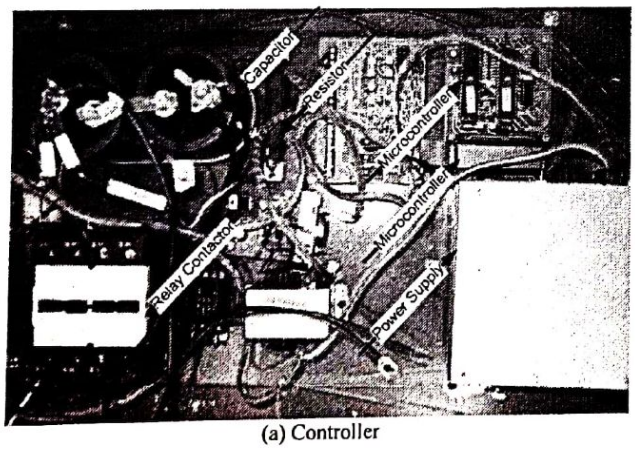
(c) Harmonic

Figs. 12. System Responses without and with the D-STATCOM

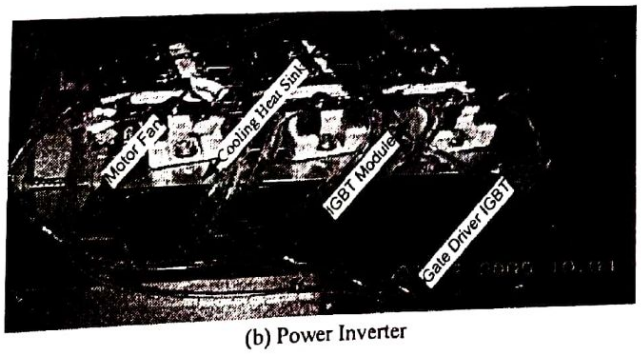
IV. Experimental Result

Figs. 13 show the experimental testing set up in the laboratory. Output of the experimental results from the 3 phase Inverter SPWM board controller is shown in Figs. 14. Fig. 15 shows the normal typical waveforms of the system voltage and current. Fig. 16 presents voltage sag typical waveforms of the system voltage and current.

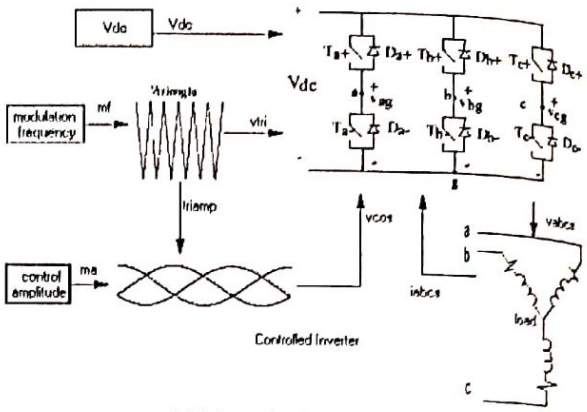
Figs. 17 show the phase-to-phase voltage during voltage sag. The duration of voltage sag is from 0.4s to 0.5s and during this period the D-STATCOM responds well to give the system better ride through capability.



(a) Controller

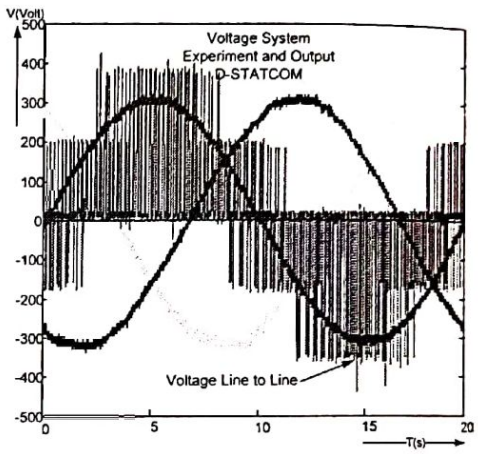


(b) Power Inverter

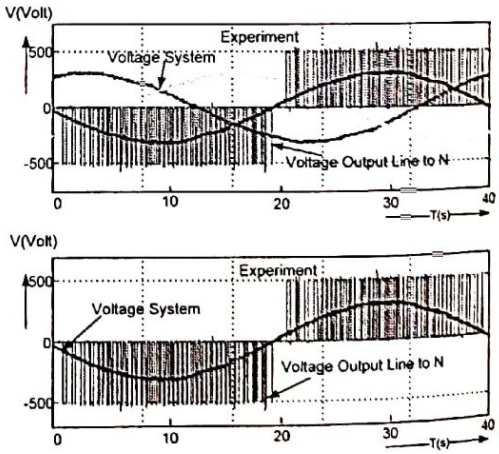


(c) Schematic of Power Inverter

Figs. 13. Laboratory Experimental Set-up



(a) System Voltage and Inverter Output Voltage L-L



(b) System Voltage and Inverter Output Voltage L- N

Figs. 14. Experimental Results of 3 Phase Output Inverter

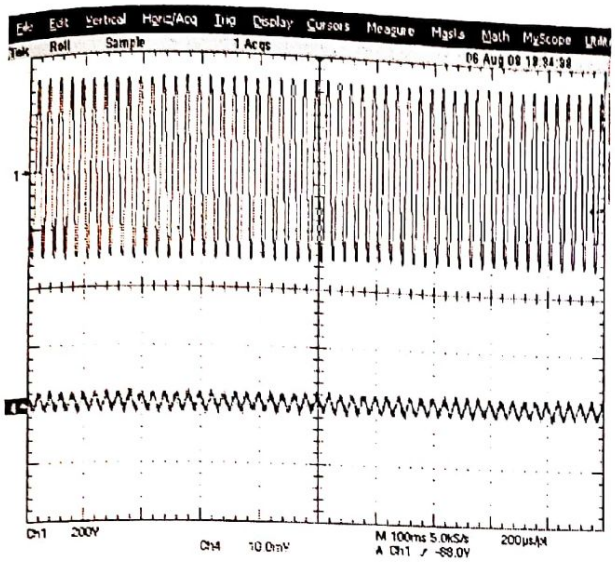


Fig. 15. Normal typical waveforms of the System Voltage and Current

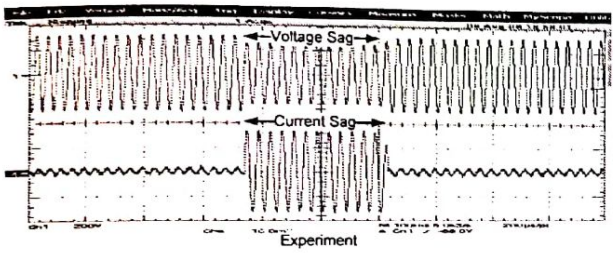
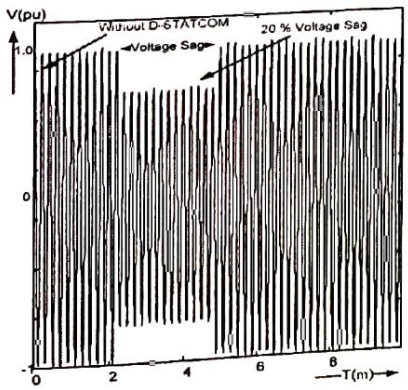
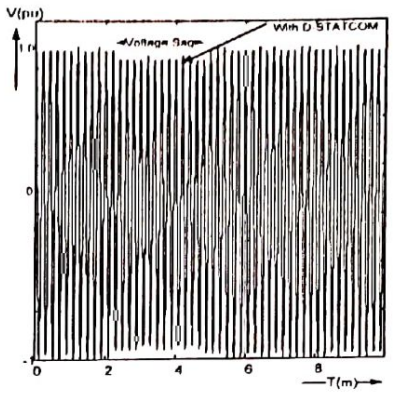


Fig. 16. Typical waveforms of the System Voltage and Current during the SLG Fault

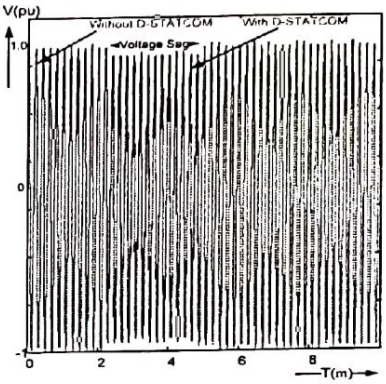
So, during the SLG fault the output voltage is as shown in Figs. 17. The measured values for line-to-line voltages are: V_{ab} = 78.1 V, V_{bc} = 125.72 V and V_{ca} = 98.72 V. The percentage unbalance can be calculated using equation (5) and found to be 20%. This value indicates that the unbalanced voltage during SLG fault is severe. Figure 18 presents the comparison of voltage sag distribution obtained from experimental measurement and simulation waveforms of the system during 20% voltage sag condition.



(a) Voltage Sag waveforms without D-STATCOM



(b) Voltage Sag waveforms with D-STATCOM



(c) Voltage Sag waveforms without and with D-STATCOM

Figs. 17. Experimental Voltage Sag Results

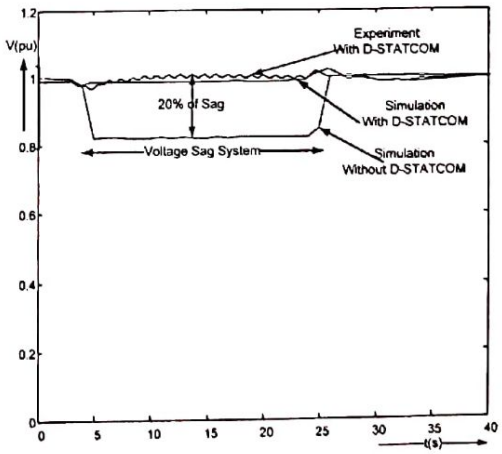


Fig. 18. Comparison of experimental measurement and simulation, typical waveforms of the system during 20% voltage sag condition

V. Conclusion

The study here presented, shows that the complete and detail model developed using PSCAD is sufficiently good for simulation. Somehow, the experimental

measurement could not be quite precise when it concerns the first microseconds of starting the D-STATCOM operation to SLG faults. On the other hand, after some microseconds the suitability between the simulation and experimental measurement curves is good.

A simulation construction of the 12-pulse D-STATCOM has been designed using the PSCAD/EMTDC program. An important aspect considered in the design is the control system. The control strategy for the D-STATCOM is the AC side voltage or reactive power control. PI controller is used to control the flow of reactive power to and from the DC capacitor. Phase Lock Loop components are used in the control to generate the switching signal, i.e. triangular waves, and reference signals, i.e. sinusoidal wave. PWM switching control is used to switch on and off the IGBT's. The IGBT's are connected inversely and parallel to the diodes for commutation purposes and to charge the capacitor. IGBTs are used in this simulation because it is easy to control the switch on and off of their gates and suitable for the designed D-STATCOM.

From the simulation results, the construction of the designed D-STATCOM responded well in mitigating voltage sag caused by SLG faults and load (source) harmonics. The DC capacitor value is dependent on the percentage of voltage sag. The difference of step drop load current during sag is the amount of reactive current needed to be compensated.

Lastly, the development of the D-STATCOM is a promising device and will be a prominent feature in power systems in mitigating power quality related problems in the near future.

Acknowledgements

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