DESIGN OF A PROTOTYPE D-STATCOM FOR VOLTAGE SAG MITIGATION

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Abstract: **This paper presents the design of a prototype distribution static compensator (D-STATCOM) for voltage sag mitigation in an unbalanced distribution system. The D-STATCOM is intended to replace the widely used static Var compensator (SVC). For fast response requirement, the feedforward compensation scheme is employed to enable the D-STATCOM to mitigate voltage sag and at the same time correct the power factor, thus acting as a load compensator. The compensation scheme of the D-STATCOM is derived using the symmetrical component method. In this work, the 12-pulse D-STATCOM configuration with IGBT has been designed and the graphic based models of the D-STATCOM have been developed using the PSCAD/EMTDC electromagnetic transient simulation program. Accordingly, simulations are first carried out to illustrate the use of D-STATCOM in mitigating voltage sag in a distribution system. Simulation results prove that the D-STATCOM is capable of mitigating voltage sag as well as improving power quality of a system.**

Keywords: *D-STATCOM, load compensation, voltage sag.*

1. Introduction

Voltage sags is the most important power quality problems faced by many industries and utilities. It contributes more than 80% of power quality (PQ) problems that exist in power systems [1]. By defintion, a voltage sag is an rms (root mean square) reduction in the AC voltage at the power frequency, for duration from a half-cycle to a few seconds [2]. Voltage sags are not tolerated by sensitive equipments used in modern industrial plants such as process controllers, programmable logic controllers (PLC), adjustable speed drive (ASD) and robotics [1]. It has been reported that, high intensity discharge lamps used for industrial illumination get extinguished at voltage sags of 20% and industrial equipments like PLC and ASD are about 10% [3].

Various methods have been applied to reduce or mitigate voltage sags. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing uninterruptible power supplies (UPS). However, the PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. The D-STATCOM has emerged as a promising device to provide not only for voltage sags mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction and harmonic control [4]. The D-STATCOM has additional capability to sustain reactive current at low voltage, reduce land use and can be developed as a voltage and frequency support by replacing capacitors with batteries as energy storage [5].

In this paper, the configuration and design of the D-STATCOM will be explained in brief. The designed D-STATCOM is connected in shunt to the 11 kV test distribution system. Passive filters will be employed to reduce the harmonics present

in the output of the D-STATCOM which exceed the limits by IEEE standards. Simulation results on the performance of the D-STATCOM for voltage sag mitigation are the shown and explained.

2. Basic Configuration and Operation of D-STATCOM

The D-STATCOM is a three-phase and shunt connected power electronics based device. It is connected near the load at the distribution systems. The major components of a D-STATCOM are shown in Figure 1. It consists of a dc capacitor, three-phase inverter (IGBT, thyristor) module, ac filter, coupling transformer and a control strategy [5]. The basic electronic block of the D-STATCOM is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency.

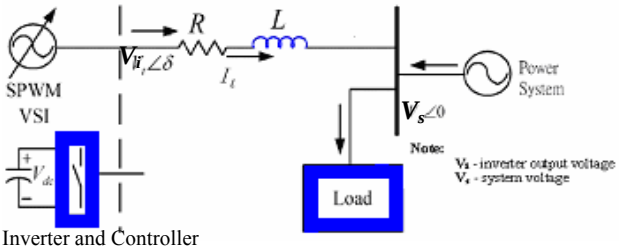
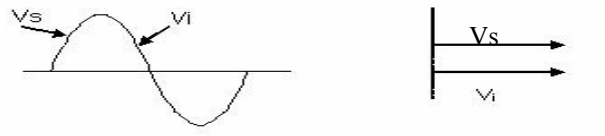
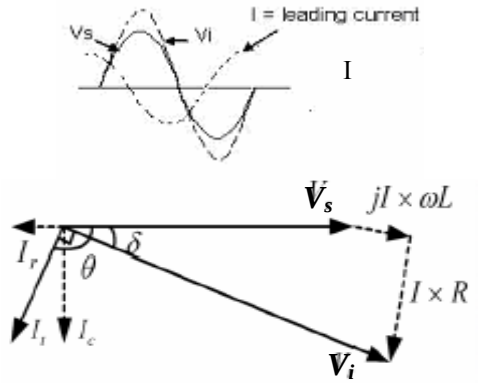


Figure 1: Basic Building Blocks of the D-STATCOM

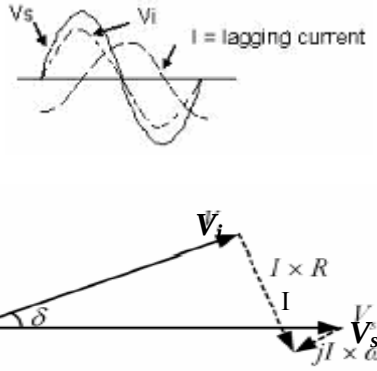
The D-STACOM employs an inverter to convert the DC link voltage V_{dc} on the capacitor to a voltage source of adjustable magnitude and phase. Therefore the D-STATCOM can be treated as a voltage-controlled source. The D-STATCOM can also be seen as a current-controlled source. Figure 1 shows the inductance L and resistance R which represent the equivalent circuit elements of the step-down transformer and the inverter will is the main component of the D-STATCOM. The voltage V_i is the effective output voltage of the D-STATCOM and δ is the power angle. The reactive power output of the D-STATCOM inductive or capacitive depending can be either on the operation mode of the D-STATCOM. Referring to figure 1, the controller of the D-STATCOM is used to operate the inverter in such a way that the phase angle between the inverter voltage and the line voltage is dynamically adjusted so that the D-STATCOM generates or absorbs the desired VAR at the point of connection. The phase of the output voltage of the thyristor-based inverter, V_i, is controlled in the same way as the distribution system voltage, V_s. Figure 2 shows the three basic operation modes of the D-STATCOM output current, I, which varies depending upon V_i. If V_i is equal to V_s, the reactive power is zero and the D-STATCOM does not generate or absorb reactive power. When V_i is greater than V_s, the D-STATCOM shows an inductive reactance connected at its terminal. The current, I, flows through the transformer reactance from the D-STATCOM to the ac system, and the device generates capacitive reactive power. If V_s is greater than V_i, the D-STATCOM shows the system as a capacitive reactance. Then the current flows from the ac system to the D-STATCOM, resulting in the device absorbing inductive reactive power [4].



a) No-load mode ($V_s = V_i$)



b) Capacitive mode ($V_i > V_s$)



c) Inductive mode ($V_i < V_s$)

Figure 2: Operation modes of D-STATCOM

3. Design of the 12-pulse D-STATCOM

Figure 3 shows a typical 12-pulse inverter arrangement utilizing two transformers with their primaries connected in series [6]. The first inverter is connected to the system through a Y-Y arrangement, whereas a Y-Δ connection is used for the second inverter. Each inverter operates as a 6-pulse inverter, with the Y-Δ inverter being delayed by 30^0 with respect to the Y-Y inverter. The current flowing into each inverter is the same, scaled by the transformer ratio, as the current being drawn from the system by the D-STATCOM. For the Y-Δ inverter, the current is also delayed by 30^0 with respect to the current of the Y-Y inverter [6].

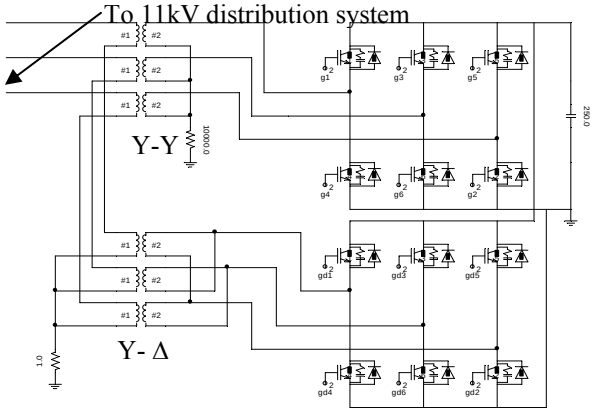


Figure 3: The 12-pulse D-STATCOM arrangement

Figure 3 also shows the proposed 12-pulse D-STATCOM configuration with the IGBT's used as power devices. The IGBTs are connected anti parallel with diodes for commutation purposes and charging of the DC capacitor [7].

The DC side of D-STATCOM is connected in parallel to keep the voltage on the DC side as low as possible and to improve utilization of the DC side capacitor. The first transformer is in wye-to-wye connection and the second transformer is in wye-to-delta connection. This is to give a 30^0 phase shift between the pulses and to reduce harmonics generated from the D-STATCOM. Both transformers are stepped down from 11kV to 2kV, i.e. 11:2 transformers. The D-STATCOM is connected in shunt to the system.

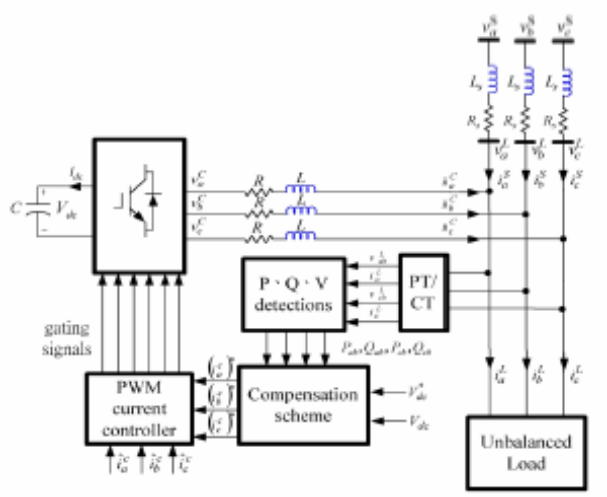


Figure 4: Shows the proposed D-STATCOM Control schema using the pulse width modulation (PWM) current controller.

3.1 Inverter Design

Inverters are used to convert DC signal to AC signal. In this work a 3-phase inverter has been developed. The DC source in the system is the DC capacitor. Which is located in parallel with the D-STATCOM.

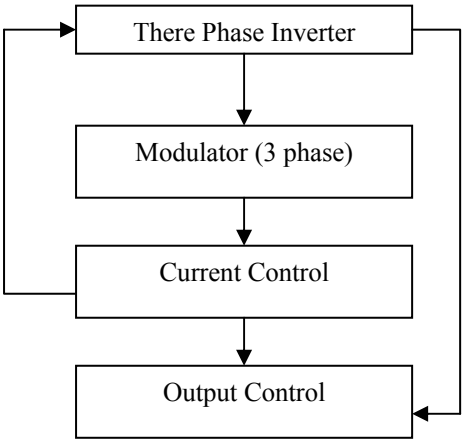


Figure 5 : Modeling of Inverter

The charging of the capacitor is referred is to the reactive power in the system. The capacitor charged when the current in the system is higher than in the D-STATCOM and is discharged when the current is lower. For inverter the most important part is the sequences of operation of the IGBTs. The IGBTs signals are referred to the Sinusoidal Pulse Width Modulation (SPWM) that will generate the pulses for the firing of the IGBTs. Figure 5 shows the modeling of the inverter.

3.2 Capacitor Sizing

Capacitor sizing is referred to the fault current in the system. The difference in current between the current before and after the fault is considered as current faults. In capacitor sizing, a suitable range of DC capacitor is needed to store the energy to mitigate the voltage sag.

The DC capacitor, C_{DC} is used to inject reactive power to the D-STATCOM when the voltage is in sag condition. In the design, the harmonic effects must be considered because the load is inductive and this may affect the value of C_{DC}. The following equation is used to calculate C_{DC} [7] ,

$$\tfrac{1}{2} C_{DC} [V_{CMAX}^2 - V_{DC}^2] = \tfrac{1}{2} V_{SM} . \Delta I_L .T \quad (1)$$

Equation (1) is used for harmonic mitigation in single phase system but for a three phase system the equation is given by,

$$C_{DC} = 3 \times \frac{V_s . \Delta I_L . T}{V_{C_{\max}}^2 - V_{DC}^2} \quad (2)$$

where,

V_S = peak phase voltage
I_L = step – drop of load current
T = period of one cycle of voltage and current
V_{CMAX} = pre-set upper limit of the energy storage C (per-phase),
V_{DC} = voltage across C (per-phase).

The value of ΔI_L can be found by measuring the load current before and during the voltage sag [7].

The value of V_{DC} is given form by

$$V_{DC} = \frac{3\sqrt{3}.V_s . \cos \alpha}{\pi} \quad (3)$$

where,

α = delay angle

if α = 0, the equation become,

$$V_{DC} = \frac{3\sqrt{3}.V_s}{\pi} \quad (4)$$

The value of V_{CMAX} is the present upper limit of C_{DC}, and is two or three times of the $V_{DC.}$

3.3 Transformer Configuration

For the 12-pulse operation, two six-pulse inverters that are shifted by 30^0 from each other can provide the phase angle shift for a suitable configuration. For the 12-pulse D-STATCOM, the transformers are connected in parallel to each other for six pulse arrangement. The first inverter is connected in Y-Y to the system lagging 30^0 from the second inverter which is connected in Y-Δ arrangement to the system. For Y-Δ connection, it will provide a phase shift of about 30^0. This phase shift is needed to make sure the operation of the 12 pulse D-STATCOM is in a stable condition.

4. Controller Configuration

The control used in the simulation is AC voltage control or reactive power control. This control is divided into two parts, that is, the sinusoidal pulse width modulation (SPWM) and reactive power control. Figure 6 shows that the PI controller regulates the AC side voltage sourced converter (VSC) or alternatively, reactive power into or

out of the VSC. The output of PI controller is the angle order, which is used to maintain the phase shift. The reactive power flow from the system is compared to the reference per-unit voltage that contributes to a change of the phase shift. The difference in phase shift will provide the needed reactive power from the DC capacitor.

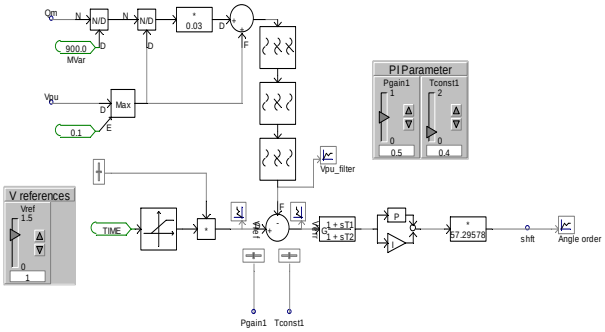


Figure 6: Reactive power Control Loop

The sinusoidal PWM (SPWM) technique is described in Figure 7 and Figure 8. The SPWM firing pulse to the IGBTs are obtained by comparing the PWM carrier signals and the reference sine waveform. The phase locked loop (PLL) plays an important role in synchronizing the switching to the distribution system voltage and lock to the phase at fundamental frequency to generate the PWM triangular carrier signals.

The frequency is multiplied with PWM switching frequency. As shown in Figure 8, the switching frequency is set at 1.5 kHz, which is 30 times the system operating frequency, and converted to a triangular signal whose amplitude is fixed between –1 to +1. In Figure 7, the pulses PLL are applied to generate sinusoidal curves at the wanted fundamental frequency. A shift is effectively the output coming from the reactive power control loop, i.e. the angle order. The difference in angle order will change the width of the PWM signal and ultimately the needed reactive power to be supplied to the system.

In this simulated, the amplitude is fixed and phase shift is control to maintain at 30^0. Figure 9 show the output of a triggering signal of IGBT when a voltage sag occurs in the system.

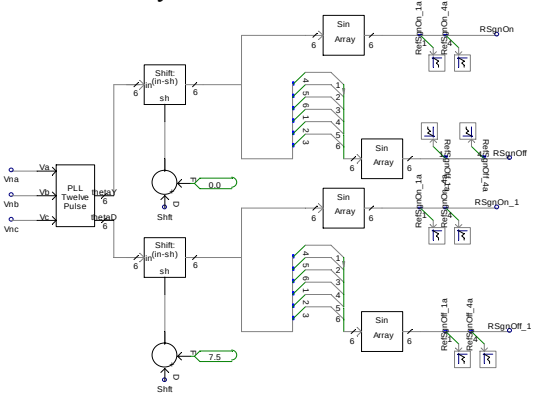


Figure 7: Generation of Reference Sine ware

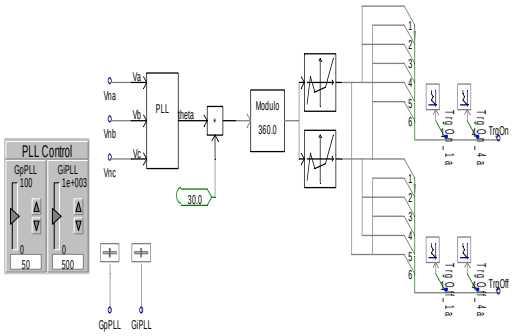


Figure 8: PWM Carrier Signal

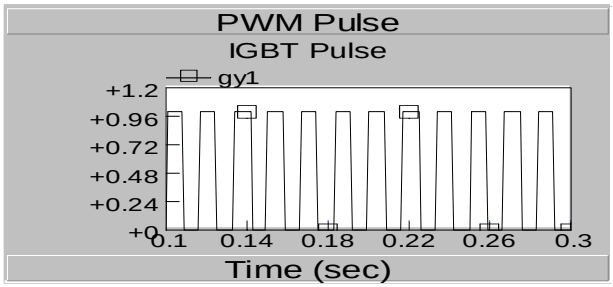


Figure 9: Simulation of IGBT pulse

5. Simulation Results and Discussion

In the simulation study, a voltage sag in the system is created by the three-phase fault component from the PSCAD/EMTDC software's library.

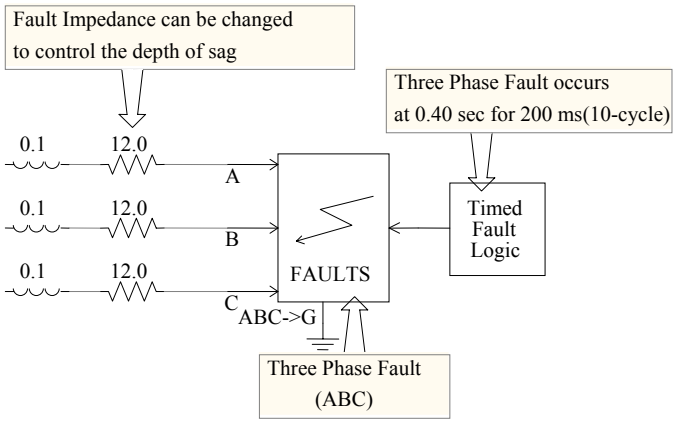


Figure 10: Three-phase Fault Component to Introduce Voltage Sag

Figure 10 shows the component applied to generate a voltage sag. The system was simulated for 0.8 seconds with a three-phase balanced fault occurring at time 0.4 sec for a duration of 0.2 sec. Figure 11 shows the per-unit voltage, current and voltage profiles of the system. From Figure 11, it can be seen that due to the three-phase fault, voltage sag has occurred. The depth of sag can be changed by changing the fault impedance.

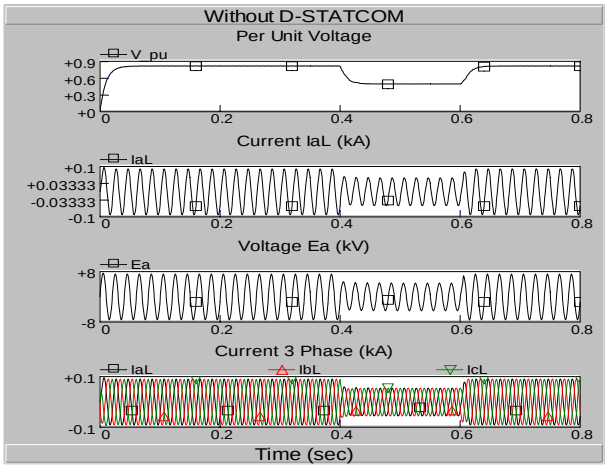


Figure 11: Voltage (p.u), Current(kA), Voltage(kV) and Three phase Current(kA)of the System during Voltage Sag Condition

The percentage of sag for the system is calculated using the following equation,

$$Sag\ (\%) = \frac{V_{pre-sag}\ (p.u) - V_{sag}\ (p.u)}{V_{pre-sag}\ (p.u)} \times 100$$
$$= \frac{0.818 - 0.498}{0.818} \times 100 \qquad (5)$$
$$= 39.12\ \%$$

It is evident from the graphs shown in Figure 11 that the line current, I_{L-L} (rms), dropped from 89A to 62A and the line voltage, V_{L-L}, dropped from 7.344kV to 4.97kV. From these values, the DC capacitor value is determined as follows (equation 2);

$$C_{DC} = 3 \times \frac{V_s . \Delta I_L . T}{V_{C_{\max}}{}^2 - V_{DC}{}^2}$$

where, in this case for V_S = 1633 V, I_L = 148.5A, T = 20ms, $V_{C_{\max}}$ = 8400V and V_{DC} = 2000V, the calculated capacitance value is $C_{DC} \approx 220\mu F$.

The VAR rating of the D-STATCOM when C_{DC}=220μF is calculated as,

$$\text{VAR} = 314.2 \times C_{DC} \times V_{L-L}^2$$

V_{L-L} is the nominal line-to-line voltage of the system at the point of connection of the filter. In this case, V_{L-L} = 6.93kVand the VAR rating of the D-STATCOM is 3.3 MVAR.

6. Mitigation of Voltage Sags by D-STATCOM

The D-STATCOM is now connected in shunt with the 11kV system and the simulation is set to run again for 0.8sec. The switching frequency of the SPWM control is set at 1.65kHz. Figure 12 and Figure 13 show the results obtained from the simulation. From Figure 12, it can be seen that the system's per unit voltage is maintained at 1.0 p.u. The spikes at the beginning and end of sag are due to capacitor charging and discharging. Figure 13 shows the duration of voltage sag from 0.4s to 0.6s and during this period the D-STATCOM responds well to give the system better ride through capability. The sag was mitigated within 20 ms and limited to less than 20% of sag before the system recovered to 1.0 p.u.

Figure 13 shows that the D-STATCOM through the control feedback, the angle order is always kept at 30^0 between the 12 pulses. It can be seen that the DC current of the DC capacitor is fluctuating from negative to positive. This is due to the capacitor charging and discharging. The primary voltage of the 11: 2 transformer, i.e. the system voltage, is maintained at about 11kV during the duration of sag. This proves that the D-STATCOM works very well in compensating the voltage sag caused by the balanced three-phase fault.

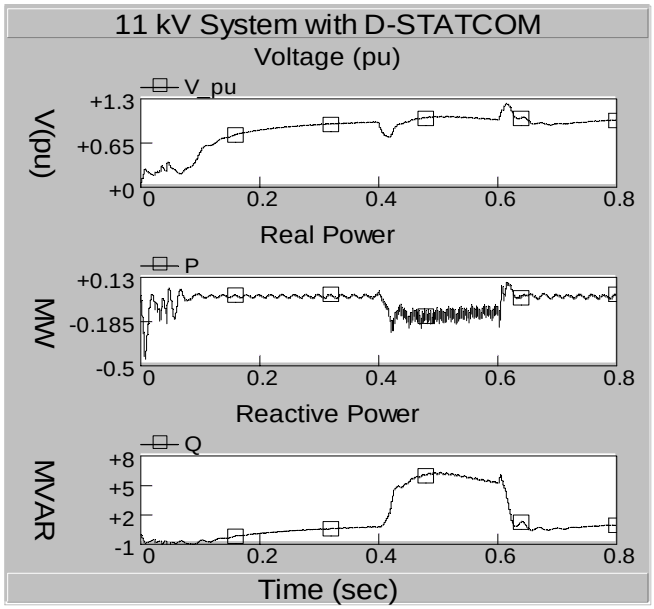


Figure 12: 11kV System with D-STATCOM : V (p.u), Real and Reactive Power

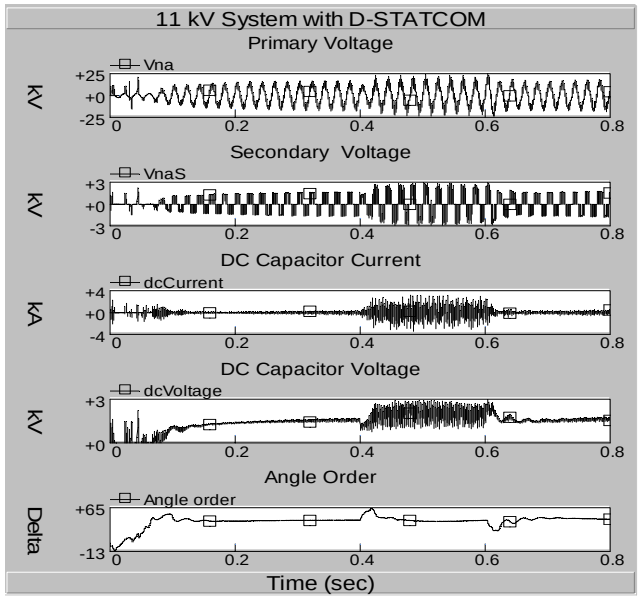


Figure 13: System Responses with the D-STATCOM

7. Conclusions

A simulation model of the 12-pulse D-STATCOM has been designed using the PSCAD/EMTDC program. An important aspect considered in the design is the control system. The control strategy for the D-STATCOM is the AC side voltage or reactive power control. PI controller is used to control the flow of reactive power to and from the DC capacitor. Phase Lock Loop components are used in the control to generate the switching signal, i.e. triangular waves, and reference signals, i.e. sinusoidal wave. PWM switching control is used to switch on and off the IGBT's. The IGBT's are connected inversely and parallel to the diodes for commutation purposes and to charge the capacitor. IGBTs are used in this simulation because it is easy to control the switch on and off of their gates and suitable for the designed D-STATCOM.

From the simulation results, the designed D-STATCOM responded well in mitigating voltage sag caused by three-phase balanced fault. The DC capacitor value is dependent on the percentage of voltage sag. The difference of step drop load current during sag is the amount of reactive current needed to be compensated.

Lastly, the D-STATCOM is a promising device and will be a prominent feature in power systems in mitigating power quality related problems in the near future.

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9. Biographies

Hendri Bin Masdi was born in West Sumatera, Indonesia. He graduated with Sarjana Teknik (Bachelor of Engineering) from Padang University, Indonesia in 1989. He obtained his Master of Technology from Bandung Institute of Technology (ITB), Indonesia in 2000. He is a PhD student at Electrical & Electronic Engineering Department, Faculty of Engineering Universiti Putra Malaysia, Malaysia since 2001.

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A Mohamed (SM) received her B.Sc. Eng. From King's College, University of London in 1978; M.Sc. and PhD (Power System), from University of Malaya, Malaysia in 1988 and 1995 respectively. This author became a Senior Member (SM) of IEEE in 2003. She is currently an professor and Head of Department at the Department of Electrical, Electronics and System Engineering, Universiti Kebangsaan Malaysia (UKM), Malaysia. Her current research interests are in power quality and other power system studies.

Sallehhudin Yusuf was born in Perak, Malaysia in 1954. After graduating from Southampton University in 1978, he worked in TNB, Malaysia for 17 years in various areas of business and engineering. He obtained MEE degree from UTM Malaysia 1989 and PhD degree from McMaster University, Canada in 1993. Salleh worked for PTI-Asia between 1995 and 2000. In November 2000, Salleh and colleagues formed Advanced Power Solutions (APS), a Strategic Global Partner of Shaw PTI. Since with APS, Salleh has been heavily involved in development and worldwide supports of Shaw PTI software products. In addition, he continues to provide consulting and educational services in the region. He is a member of CIGRE and the IEEE and currently the Vice-Chair of IEEE PES Chapter Malaysia.