Design of a Prototype D-Statcom using DSP Controller for Voltage Sag Mitigation

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Abstract-- **This paper presents the design of a prototype distribution static compensator (D-STATCOM) for load compensation in an unbalanced distribution system. The D-STATCOM is intended to replace the widely used static Var compensator (SVC). The compensation scheme of the D-STATCOM is derived using the symmetrical component method. In this work, the 12-pulse D-STATCOM configuration with IGBT has been designed and the graphic based models of the D-STATCOM have been developed using the PSCAD/EMTDC electromagnetic transient simulation program. Accordingly, simulation is first carried out to illustrate the use of D-STATCOM in mitigating voltage sag in a distribution system. The D-STATCOM has been developed using DSP controller to achieve excellent overall performance. Simulation results prove that the D-STATCOM is capable of mitigating voltage sag by controlling PWM of the system using DSP board.**

Index Terms-- **D-Statcom, load compensation, voltage sag.**

I. INTRODUCTION

VOLTAGE sags is the most important power quality problems faced by many industries and utilities. It contributes more than 80% of power quality (PQ) problems that exist in power systems [1]. By definition, a voltage sag is an rms (root mean square) reduction in the AC voltage at power frequency, for duration from a half-cycle to a few seconds [2]. Voltage sags are not tolerated by sensitive equipment used in modern industrial plants such as process controllers; programmable logic controllers (PLC), adjustable speed drive (ASD) and robotics [1]. It has been reported that, high intensity discharge lamps used for industrial illumination get extinguished at voltage sags of 20% and industrial equipments like PLC and ASD are about 10% [3].

Various methods have been applied to reduce or mitigate voltage sags. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing uninterruptible power supplies (UPS). However, the PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. The D-STATCOM has emerged as a promising device to provide not only for voltage sag mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction and harmonic control [4]. The D-STATCOM has additional capability to sustain reactive current at low voltage, reduced land use and can be developed as a voltage and frequency support by replacing capacitors with batteries as energy storage [5].

In this paper, the configuration and design of the D-STATCOM will be explained in brief. The designed D-STATCOM is connected in shunt to a study 11 kV distribution system. Passive filters be employed to reduce the harmonics present in the output of the D-STATCOM which exceed the limits by IEEE standards. Simulation results on the performance of the D-STATCOM for voltage sag mitigation will be shown and explained.

II. CONFIGURATION AND OPERATION OF D-STATCOM

A. Basic Configuration and Operation of D-Statcom

The D-STATCOM is a three-phase and shunt connected power electronics based device. It is connected near the load at the distribution systems. The major components of a D-STATCOM are shown in Figure 1. It consists of a dc capacitor, three-phase inverter (IGBT, thyristor) module, ac filter, coupling transformer and a control strategy [5]. The basic electronic block of the D-STATCOM is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency.
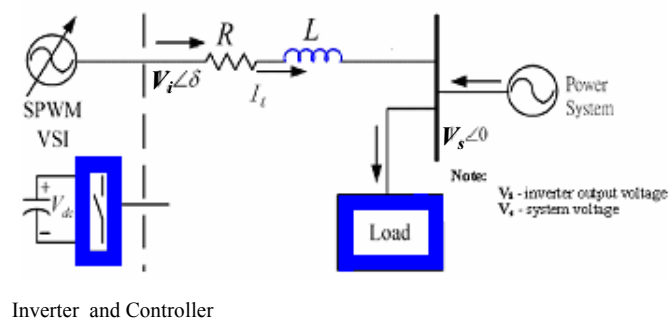

Fig. 1. Basic Building Blocks of the D-STATCOM.

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Referring to figure 1, the controller of the D-STATCOM is used to operate the inverter in such a way that the phase angle between the inverter voltage and the line voltage is dynamically adjusted so that the D-STATCOM generates or absorbs the desired VAR at the point of connection. The phase of the output voltage of the thyristor-based inverter, V_i, is controlled in the same way as the distribution system voltage, V_s. Figure 2 shows the three basic operation modes of the D-STATCOM output current, I, which varies depending upon V_i. If V_i is equal to V_s, the reactive power is zero and the D-STATCOM does not generate or absorb reactive power. When V_i is greater than V_s, the D-STATCOM 'sees' an inductive reactance connected at its terminal. Hence, the system 'sees' the D-STATCOM as a capacitive reactance. The current, I, flows through the transformer reactance from the D-STATCOM to the ac system, and the device generates capacitive reactive power. If V_s is greater than V_i, the system 'sees' an inductive reactance connected at its terminal and the D-STATCOM 'sees' the system as a capacitive reactance. Then the current flows from the ac system to the D-STATCOM, resulting in the device absorbing inductive reactive power [4].

a) No-load mode (Vs = Vi)

b) Capacitive mode (Vi >Vs)
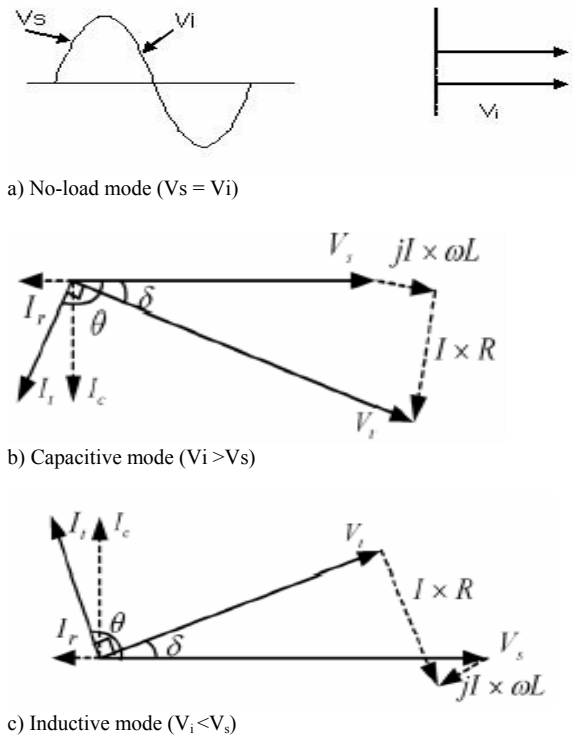

c) Inductive mode (V_i<V_s)

Fig. 2. Operation modes of D-STATCOM.

Figure 3 shows a typical 12-pulse inverter arrangement utilizing two transformers with their primaries connected in series [6]. The first inverter is connected to the system through a Y-Y arrangement, whereas a Y-Δ connection is used for the second inverter. Each inverter operates as a 6-pulse inverter, with the Y-Δ inverter being delayed by 30^0 with respect to the Y-Y inverter. The current flowing into each inverter is the same, scaled by the transformer ratio, as the current being

drawn from the system by the D-STATCOM. For the Y-Δ inverter, the current is also delayed by 30^0 with respect to the current of the Y-Y inverter [6].
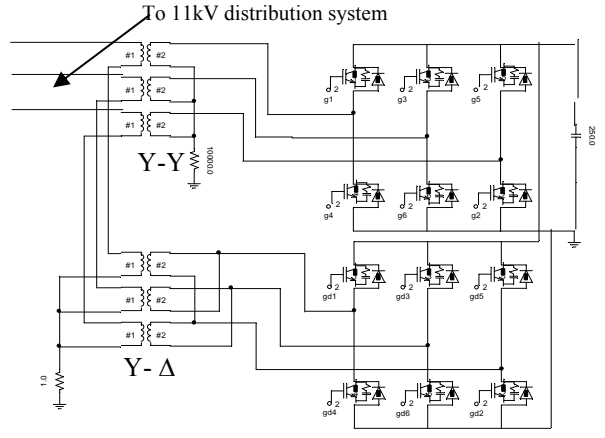

Fig. 3.   The 12-pulse D-STATCOM arrangement.

B. Design of the 12-pulse D-Statcom and Control System

Figure 4 shows the proposed 12-pulse D-STATCOM configuration with the IGBTs used as power devices. The IGBTs are connected anti parallel with diodes for commutation purposes and charging of the DC capacitor [7]. The DC side of D-STATCOM is connected in parallel to keep the voltage on the DC side as low as possible and to improve utilization of the DC side capacitor. The first transformer is in wye-to-wye connection and the second transformer is in wye-to-delta connection. This is to give a 30^0 phase shift between the pulses and to reduce harmonics generated from the D-STATCOM. Both transformers are stepped down from 11kV to 2kV, i.e. 11:2 transformers. The D-STATCOM is connected in shunt to the system.
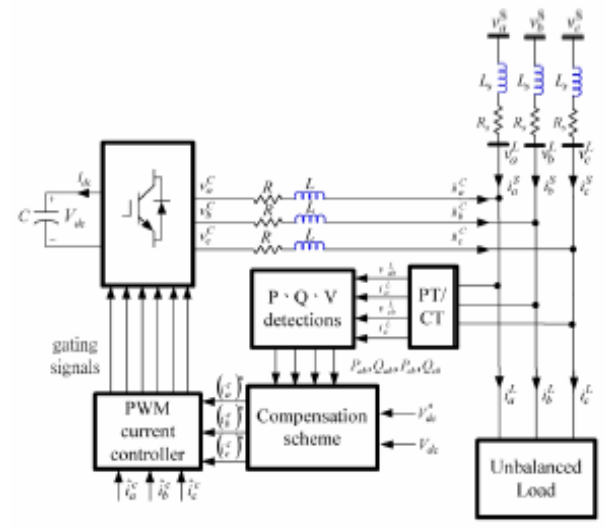

Fig. 4. The Proposed D-STATCOM Configuration.

C. InverterDesign

Inverters are used to convert DC signal to AC signal. In

this research a 3 phase inverter had been developed. The DC source in this system is the DC capacitor. It is located parallel to the D-STATCOM.

The charging of this capacitor is referred to the reactive power in the system. The capacitor charge when the current at the system higher in the D-STATCOM and will discharge when the current at D-STATCOM is lower then at the system. For inverter the most important part is the sequences of operation of the IGBTs. These IGBTs signals are referred to the SPWM that will generate the pulses for the firing of the IGBTs.

D. Capacitor sizing

Capacitor sizing is referred to the fault current in the system. The different current between the current before and after the fault is considered as current faults. In capacitor sizing the suitable range of DC capacitor is needed to store the energy to mitigate the voltage sag. The passive elements are the distribution R and L, and the DC capacitor C_{DC}. C_{DC} is used, to inject reactive power to the D-STATCOM when the distribution in sag condition. In the design the harmonic effects must be considered because the loads are inductive and this had effect in the value of C_{DC}. The following equation is used to calculate C_{DC} [7],

$$\tfrac{1}{2} C_{DC} [V_{CMAX}^2 - V_{DC}^2] = \tfrac{1}{2} V_{SM} . \Delta I_L .T \qquad (1)$$

This formula is used for harmonic mitigation in single phase system but for the three phase system the equation is given by,

$$C_{DC} = 3 \times \frac{V_s . \Delta I_L .T}{V_{C_{max}}^2 - V_{C_r}^2} \qquad (2)$$

where,

V_s = peak phase voltage,

I_L = step − drop of load current,

T = Period of one cycle of voltage and current,

$V_{C_{max}}$ = pre − set upper limit of the energy

storage C (per - phase),

V_{C_r} = voltage across C (per - phase)

The value of ΔI_L can be found by measuring the load current before and during the voltage sag. The value of V_{DC} can be form by [7]

$$V_{DC} = \frac{3\sqrt{3}.V_s . \cos \alpha}{\pi} \qquad (3)$$

where,
V_S = Peak Phase Voltage
α = Delay Angle

if α = 0, the equation become,

$$V_{DC} = \frac{3\sqrt{3}.V_s}{\pi} \qquad (4)$$

The value of V_{CMAX} is the present upper limit of C_{DC}, can be two or three times of the V_{DC}.

E. Transformer configuration

For 12-pulse operation, two six-pulse inverters, shifted by 30^0 from each other can provide the phase angle for suitable configuration. For 12-pulse D-STATCOM, the transformers are connected in parallel to each other for six pulse arrangement. The first inverter is connected in Y-Y to the system with lagging 30^0 to second inverter that is connected in Y-Δ arrangement. For Y-Δ connection it will provide phase shift of about 30^0. This phase shift is needed to make sure the operation of 12- pulse D-STATCOM is in a stable condition. The arrangements are shown below.

III. CONTROLLER CONFIGURATION

A. Microcomputer based controller (Software)

In the simulation study, the voltage sags introduced to the system was done by the three-phase fault component from the PSCAD/EMTDC software's library.
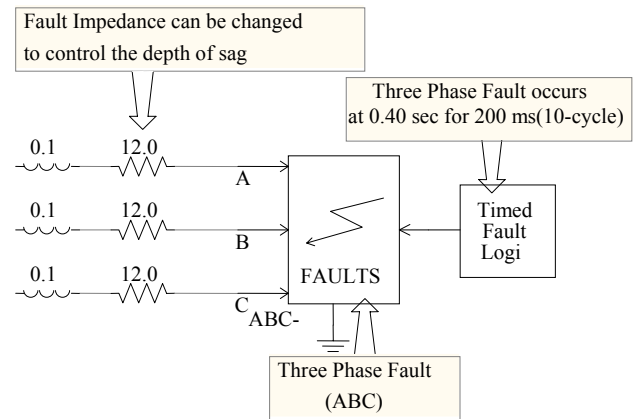

Fig. 5. Three-phase Fault Component to Introduce Voltage Sag.

Figure 5 shows, the component applied to generate voltage sag. The system was simulated for 0.8 seconds with the three-phase balanced fault occurring at time 0.4 sec for a duration of 0.2 sec. Figure 6 shows the output of triggering signal of IGBT when the voltage sag occurs in the system. Figure 7 shows the per-unit voltage, current and voltage profiles of the system. From Figure 8, we can see that due to the three-phase fault, voltage sag has occurred. The depth of sag can be changed by changing the fault impedance shown in Figure 8.
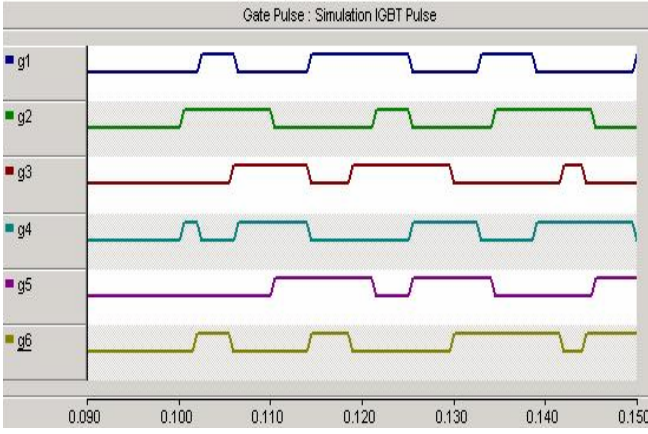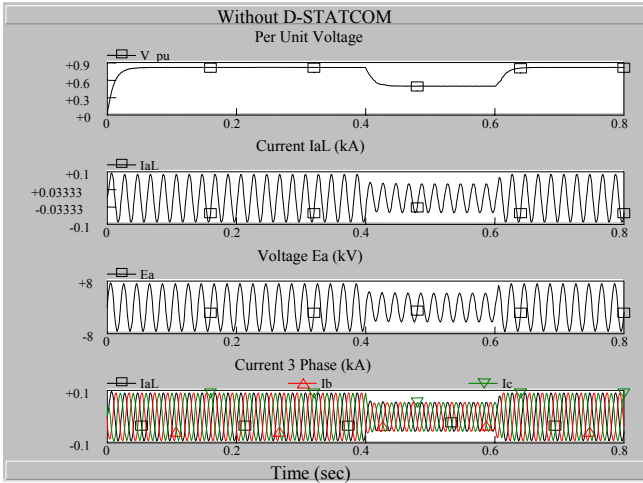
Fig. 6. Simulation of IGBT pulse.

Fig. 7. Voltage (p.u), Current(kA), Voltage(kV) and Three phase Current(kA)of the System during Voltage Sag Condition.

The percentage of sag for the system is calculated using the following equation,

$$Sag\ (\%)\ =\ \frac{V_{pre-sag}\ (p.u) - V_{sag}\ (p.u)}{V_{pre-sag}\ (p.u)} \times 100$$
$$=\ \frac{0.818\ -\ 0.498}{0.818} \times 100 \qquad (5)$$
$$=\ 39.12\ \%$$

It is evident from the graphs shown in figure 7 that the line current, I_{L-L} (rms), drops from 89A to 62A and the line voltage, V_{L-L}, drops from 7.344kV to 4.97kV. From these values, the DC capacitor value is determined using equation 2 as follows;

$$C_{DC} = 3 \times \frac{V_s.\Delta I_L.T}{V_{C_{max}}^2 - V_{C_r}^2}$$

where, in this case for V_S = 1633 V, I_L = 148.5A, T = 20ms, $V_{C_{max}}$ = 8400V and V_{C_r} = 2000V, the calculated capacitance value is $C_{DC} \approx 220\mu F$.

The VAR rating of the D-STATCOM when C_{DC}=220μF is calculated as,

$$VAR = 314.2 \times C_{DC} \times V_{L-L}^2$$

V_{L-L} is the nominal line-to-line voltage of the system at the point of connection of the filter. For this case, V_{L-L} = 6.93kV. The VAR rating of the D-STATCOM is 3.3 MVAR.
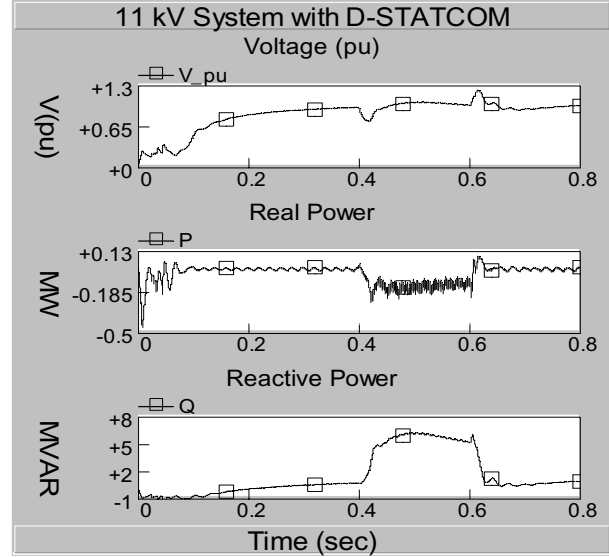

Fig. 8. 11kV System with D-STATCOM : V (p.u), Real and Reactive Power.

B. DSP Based Controller

New classes of DSP controllers are becoming a viable option for even the most cost sensitive applications like appliances, HVAC systems. In addition to traditional mathematical function like digital filter, FFT implementation this new class of DSPs integrates all the important power electronic peripherals to simplify the overall system implementation. This integration lower the over all part of the system and reduces boar size. It is used to implement a three-phase DC–AC inverter with multiple functions. These functions include the controller for generating PWM by closed loop speed control, input power factor correction. For this DSP the three-phase inverter utilizes six PWM channels for three phase inverter. The dead band is generated using the on-chip software programmable dead band. A twenty five teeth sprocket provides the speed input to the controller capture unit. Power factor correction is implemented using the well known boost topology. The power switch of the boost converter is controlled using another PWM channel of the controller [9]. Simple voltage divider circuits are used to condition and feed various voltage voltages to the analog-to-digital module of the controller. The complete driver utilizes mainly three software modules. These modules are closed loop space vector PWM. Power factor correction module is to improve the input power factor of the system and the serial communication module. The D-STATCOM and DSP block diagram is shown in figure 9 DSP board controller.
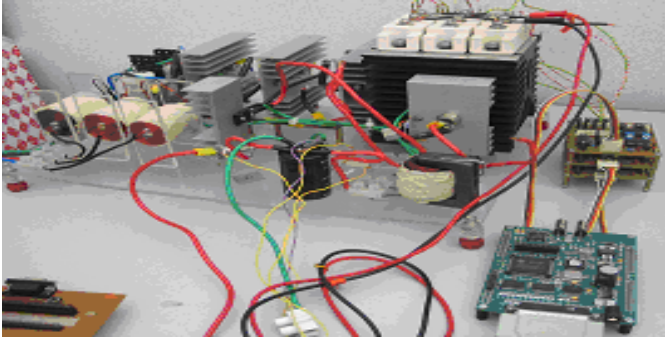
Fig. 9. The D-STATCOM and DSP board controller.

Fig. 11. Typical waveforms of inverter voltages input and currents output.

IV. EXPERIMENTAL RESULTS DSP BOARD CONTROLLER

Output experimental results the DSP board controller is shown in Figure 10 Output gate drivers, Figure 11 typical waveforms of inverter voltages, current and Figure 12 phase-to-phase voltage and phase current 100 V/div(top), 12.5 A/div(bottom), 2.0 ms/div and Fundamental frequency 60 Hz.
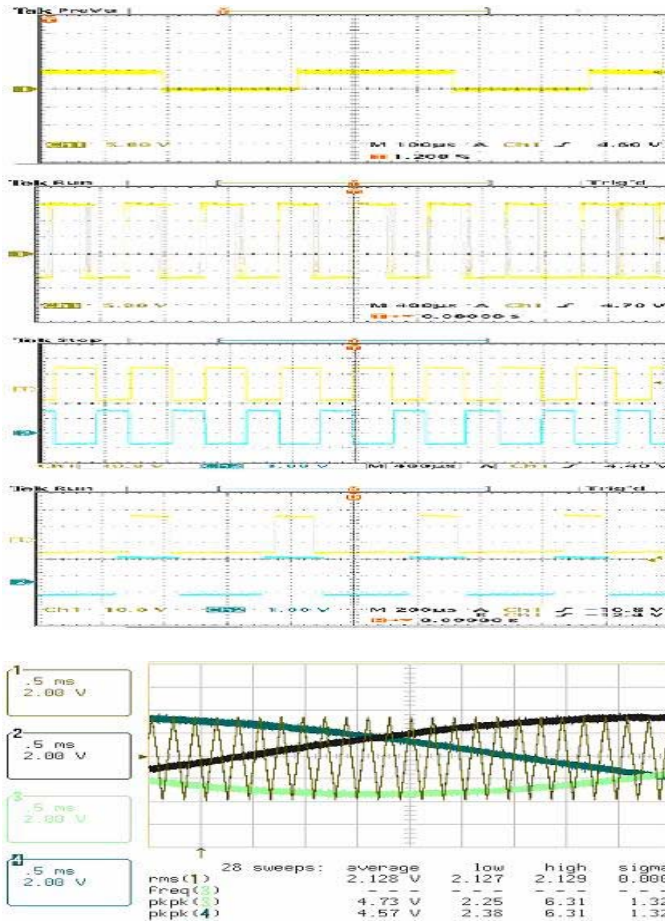

Fig. 12. Phase-to-phase Voltage and phase current.
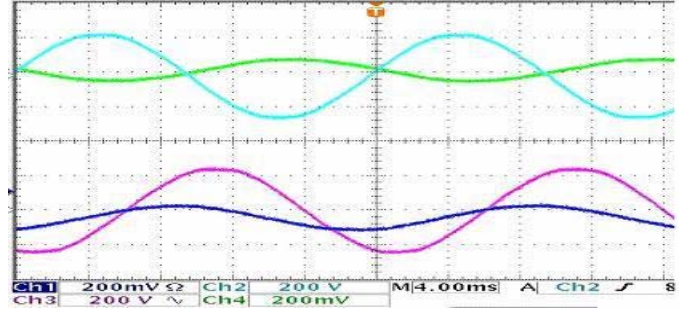

Fig. 10. Output of gate drive using DSP.
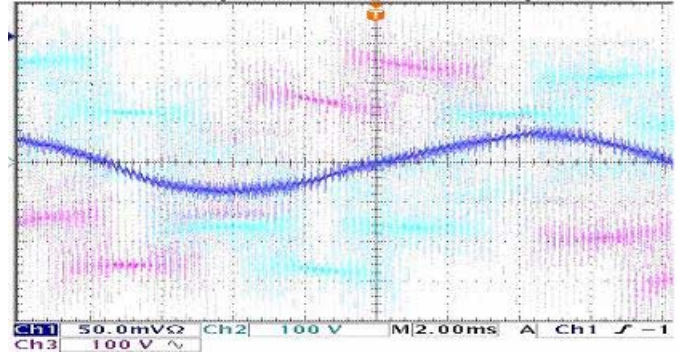
V. CONCLUSION

A simulation model of the 12-pulse D-STATCOM has been designed using the PSCAD/EMTDC program. An important aspect considered in the design is the control system. The control strategy for the D-STATCOM was the AC side voltage or reactive power control. PI controller is used to control the flow of reactive power to and from the DC capacitor. Phase Lock Loop components were used in the control to generate the switching signal, i.e. triangular waves, and reference signals, i.e. sinusoidal wave. PWM switching control was used to switch on and off the IGBTs. The IGBTs were connected inversely and parallel to the diodes for commutation purposes and to charge capacitor. IGBTs are used in this simulation because it is easy to control the switch on and off of their gates and suitable for the designed D-STATCOM system.

From the simulation results, the designed D-STATCOM responded well in mitigating voltage sag caused by three-phase balanced fault. The DC capacitor value is dependent on the percentage of voltage sag. The difference of step drop load current during sag is the amount of reactive current needed to be compensated.

In the traditional power transmission system , controllable devices are restricted to the slow mechanisms such as transformer tap changers and switched capacitor. In the late 1980's, thanks to the major developments in the semiconductor technology, it became possible to apply power electronics in the control of D-STATCOM. Based on the

above analysis, it can be conclude that there is still a room for improvement in the modeling and control DSP of the three-phase SPWM power converters.

Also, the drives used at the site are 12-pulse type causing significant harmonic current to flow from the distribution system. Because of the higt bandwidth of the D-STATCOM it can be used to inject a compensating current into the distribution network which will provide the harmonic currents drawn by the non-linear load and so help to maintain a sinusoidal voltage at the point of common coipling.

Lastly, the D-STATCOM is a promising device and will be a prominent feature in power systems in mitigating power quality related problems in the near future.

VI. ACKNOWLEDGMENT

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VIII. BIOGRAPHIES

Norman Bin Mariun, graduated from University of Nottingham, UK in Electrical and Electronic Engineering (1980), received MSc from North Carolina State University, USA (1983), and PhD from University of Bradford, UK (1998). He is Head of Department and an Associate Professor at Electrical and Electronic Engineering Department, UPM. His areas of interest include; power system quality and energy management, power electronics applications in power system and electrical drives, modelling and testing of power semiconductor devices, and application of multimedia in Engineering Education. He is a Senior Member of IEEE and a registered Professional Engineer, and the Vice-Chair of IEEE PELS-IAS-IES Malaysia Chapter and Past Chair of IEEE PES Malaysia Chapter.

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Sallehhudin Yusuf was born in Perak, Malaysia in 1954. After graduating from Southampton University in 1978, he worked in TNB, Malaysia for 17 years in various areas of business and engineering. He obtained MEE degree from UTM Malaysia 1989 and PhD degree from McMaster University, Canada in 1993. Salleh worked for PTI-Asia between 1995 and 2000. In November 2000, Salleh and colleagues formed Advanced Power Solutions (APS), a Strategic Global Partner of Shaw PTI. Since with APS, Salleh has been heavily involved in development and worldwide supports of Shaw PTI software products. In addition, he continues to provide consulting and educational services in the region. He is a member of CIGRE and the IEEE and currently the Vice-Chair of IEEE PES Chapter Malaysia.